IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A random number generator, comprising:

a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a count value of the clock signal with respect to a transition of the random signal; and

a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal,

wherein the counter circuit is a one-bit counter, the count value of which alternates between a high level and a low level every one count, the counter circuit having a clock enable input through which said random signal is supplied, and wherein when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller.

2. (Previously Presented) The random number generator of claim 1, wherein the random signal manifests a characteristic in which power spectrum intensity varies with an increase of frequency.

3. (Canceled).

4. (Original) The random number generator of claim 1, further comprising a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal.

5. (Original) The random number generator of claim 4, wherein the frequency of the random number acquisition clock is lower than the frequency of the random signal.

6. (Original) The random number generator of claim 4, wherein the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level.

7. (Original) The random number generator of claim 1, wherein a pulse counter is accessible by the clock enable input, and the output of the pulse counter becomes the random signal.

8. (Original) The random number generator of claim 1, further comprising an inverter connected between the clock enable input side and a clock input side of the first latch circuit.

9. (Canceled).

10. (Original) The random number generator of claim 1, wherein the first latch circuit is a D type flip-flop.

11. (Withdrawn) A random number generator comprising:

an AND circuit configured to be supplied with a random signal and a clock signal, and to generate a logic product of the random signal and the clock signal;

a dividing latch circuit configured to provide alternately a high level signal and a low level signal with respect to the logic product output; and

a first latch circuit configured to latch the count value with respect to a transition of the random signal, and to provide a random number signal.

12. (Withdrawn) The random number generator of claim 11, wherein the random signal manifests a characteristic in which power spectrum intensity varies with an increase of frequency.

13. (Withdrawn) The random number generator of claim 11, wherein the random signal manifests a characteristic in which power spectrum intensity decreases with an increase of frequency.

14. (Withdrawn) The random number generator of claim 11, further comprising a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal.

15. (Withdrawn) The random number generator of claim 14, wherein the frequency of the random number acquisition clock is lower than the frequency of the random signal.

16. (Withdrawn) The random number generator of claim 14, wherein the transition of the random number acquisition clock signal represents a leading edge of the random

number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level.

17. (Withdrawn) The random number generator of claim 11, further comprising a pulse counter being accessible by the clock enable input, wherein the output of the pulse counter becomes the random signal.

18. (Withdrawn) The random number generator of claim 11, wherein a period of the clock signal is less than a half of a on-state zone Tz which is obtained by subtracting a minimum on-state pulse width Tmin from a maximum on-state pulse width Tmax.

19. (Withdrawn) The random number generator of claim 11, further comprising an inverter connected between the first input side and a clock input side of the first latch circuit.

20. (Withdrawn) The random number generator of claim 11, wherein the first latch circuit is a J-K type flip-flop.

21. (Canceled).

22. (Currently Amended) A random number generator, comprising:

a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a counter value of the clock signal with respect to a transition of the random signal;

a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal; and

a source for the random signal adapted to produce said random signal having a characteristic in which power spectrum intensity decreases with increasing frequency,

wherein the source comprises an oscillation circuit using a delay time of a CR delay circuit, and wherein random variations of the resistance and capacitor values of the CR delay circuit are used for generating the random signal, and wherein when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller.

23. (Previously Presented) The random number generator of claim 22, further comprising a second latch circuit configured to receive a random number acquisition clock signal having a constant period and the first random number signal, to latch the first random number signal with respect to a transition of the random number acquisition clock signal, and to provide a second random number signal.

24. (Previously Presented) The random number generator of claim 23, wherein the frequency of the random number acquisition clock is lower than the frequency of the random signal.

25. (Previously Presented) The random number generator of claim 23, wherein the transition of the random number acquisition clock signal represents a leading edge of the random number acquisition clock signal when the random number acquisition clock signal changes from a low level to a high level.

26. (Previously Presented) The random number generator of claim 22, wherein a pulse counter is accessible by the clock enable input, and the output of the pulse counter becomes the random signal.

27. (Previously Presented) The random number generator of claim 22, further comprising an inverter connected between the clock enable input side and a clock input side of the first latch circuit.

28. (Previously Presented) The random number generator of claim 22, wherein the first latch circuit is a D type flip-flop.

29. (New) A random number generator, comprising:

a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a count value of the clock signal with respect to a transition of the random signal; and

a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal,

wherein the counter circuit is one-bit counter, the counter value of which alternates between a high level and low level every one count, the counter circuit having a clock enable input through which said random signal is supplied, and wherein when a period of the clock signal is smaller, a frequency of each occurrence of "0" and "1" becomes closer to 0.5.

30. (New) A random number generator, comprising:

a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a counter value of the clock signal with respect to a transition of the random signal;

a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal; and

a source for the random signal adapted to produce said random signal having a characteristic in which power spectrum intensity decreases with increasing frequency,

wherein the source comprises an oscillation circuit using a delay time of a CR delay circuit, and wherein random variations of the resistance and capacitor values of the CR delay circuit are used for generating the random signal, and wherein when a period of the clock signal is smaller, a frequency of each occurrence of "0" and "1" becomes closer to 0.5.